AMENDMENT TO THE CLAIMS

Please add claims 20-38 as follows:

20. (New) A system, comprising:

a first serial device having n ports, each port supporting a serial communications path; and

an arbitration-and-control apparatus configured to arbitrate for control of the serial communications path and, after control is achieved, maintain control of the serial communications path as long as at least a first predetermined amount of data is available within control of the first serial device, wherein the first predetermined amount of data within control of the first serial device includes at least some data not available for transfer to the serial communications path.

21. (New) The system of claim 20 wherein n comprises one or more.

22. (New) The system of claim 20, further comprising:

a serial device circuit chip, the chip having an on-chip data buffer, wherein the first predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the serial communications path; and

an off-chip memory, wherein the first predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the serial communications path but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

23. (New) The system of claim 22, wherein the predetermined amount of on-chip data includes a programmable amount of data.

24. (New) The system of claim 22, wherein the predetermined amount of off-chip data includes a programmable amount of data.

25. (New) The system of claim 22, wherein the predetermined amount of on-chip data includes a programmable amount of data, the predetermined amount of off-chip data includes a programmable amount of data, and the predetermined amount of off-chip data is a different amount than the predetermined amount of on-chip data.

26. (New) The system of claim 25, further comprising:

a data storage device operatively coupled to the first serial device; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in order to transfer data between the first and second serial devices through the serial communications path.

27. (New) The system of claim 20, wherein the arbitration-and-control apparatus, for at least one transfer operation, delays the start of the transfer operation until after a second predetermined amount of data is available for transfer.

28. (New) The system of claim 20, further comprising:

a serial device circuit chip, the chip having an on-chip data buffer; and

an off-chip memory operatively coupled to supply data to the serial device circuit chip, wherein the communications path is held open if at least one-half a packet of data is contained in the on-chip data buffer, and at least one packet of data are contained in off-chip memory.

29. (New) A data storage system, comprising:

a storage medium;

a serial device having n ports, each port supporting a serial communications path that carries a data protection code within data transmissions on the serial communications path, the serial device operatively coupled to communicate data to and from the storage medium; and

an arbitration-and-control apparatus operatively coupled to the serial device to reduce connection overhead, wherein the arbitration-and-control apparatus arbitrates for control of the serial communications path and, after control is achieved, maintains control of the serial communications path as long as at least a first predetermined amount of data is available within control of the serial device, wherein the first predetermined amount of data within control of the serial device includes at least some data not available for transfer to the serial communications path.

30. (New) The data storage system according to claim 29, further comprising:

a serial device circuit chip within the serial device, the chip having an on-chip data buffer, wherein the predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the serial communications path; and

an off-chip memory, wherein the predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the serial communications path but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

31. (New) A method, comprising:

arbitrating for control of a serial communications path; and

maintaining control of the serial communications path as long as a first predetermined minimum amount of data is available within control of a first serial device, wherein the first predetermined amount of data within control of the first serial device includes at least some data not currently available for transfer to the serial communications path.

32. (New) The method according to claim 31, wherein maintaining control further comprises:

determining an on-chip amount of data available in a serial device circuit chip;

determining an off-chip amount of data available in an off-chip memory;

comparing the on-chip amount of data available to a predetermined minimum-required amount of on-chip data;

comparing the off-chip amount of data available to a predetermined minimum-required amount of off-chip data; and

maintaining control of the serial communications path based on the comparisons.

33. (New) The method according to claim 32, wherein maintaining control of the serial communications path as long as a first predetermined minimum amount of data is available, further comprises:

programmably changing the predetermined minimum-required amount of on-chip data and the predetermined minimum-required amount of off-chip data.

34. (New) The method according to claim 32, wherein maintaining control of the serial communications path as long as a first predetermined minimum amount of data is available, further comprises:

programmably changing the predetermined minimum-required amount of off-chip data to a different amount than the predetermined minimum-required amount of on-chip data.

35. (New) The method according to claim 32, wherein maintaining control of the serial communications path as long as a first predetermined minimum amount of data is available, further comprises:

programmably changing the predetermined minimum-required amount of off-chip data.

36. (New) The method according to claim 31, further comprising:

transferring data through the serial-communications path between a data storage device that is operatively coupled to the first serial device and a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device by the serial-communications path.

37. (New) The method according to claim 31, further comprising:

beginning a transfer operation only after a second predetermined amount of data is available for transfer.

38. (New) A system, comprising:

a first serial device having n ports, each port supporting a serial communications path, each serial communications path including a data protection code within data transmissions on the serial communications path; and

arbitration-and-control means for arbitrating for control of

the serial communications path and, after control is achieved, maintaining control of the serial communications path as long as at least a first predetermined amount of data is available within control of the serial device, wherein the first predetermined amount of data within control of the serial device includes at least some data not available for transfer to the serial communications path.